L18: Entry 32 of 39 File: USPT Aug 13, 2002

DOCUMENT-IDENTIFIER: US 6431182 B1
TITLE: Plasma treatment for polymer removal after via etch

Detailed Description Text (6):
In another application of the process invention, the semiconductor device 34 includes borderless vias 40 as shown in FIGS. 5 and 6 after a typical prior art etch step and removal of the photoresist strip. These borderless vias 40 also exhibit the same problem as described hereinbefore for the vias 20 having borders. As shown in FIG. 5, the organometallic deposit 28 is formed on the interlayer dielectric layer 22 and the metal line 31. In FIG. 6, the organometallic deposit 28 is formed on the layer 22, the metal line 31 and another low-k dielectric HSQ layer 42. Upon application of the cleaning process of the invention, the organometallic deposit is removed, leaving a clean form of the borderless vias 40.

Detailed Description Text (7):
The process of the invention is generally compatible with low-k dielectric materials. The dielectric layer 38 in the via, which is etched by the process of the present invention, is typically TEOS or other low-k dielectrics such as hydrogen silsesquioxide (HSQ), either alone or in combination. In one typical application of the process, the via 20 is cleaned by applying reactive ion etching with water vapor supplying oxygen with a voltage bias applied to the plasma 21. The fluorine-based constituent used was tetrafluoromethane, and a bias power was also applied. The result of the processing was a clean form of the via 20 with a minimum of visible breakdown and detected porosity of the sidewall 38 of the via 20 after cleaning.

Detailed Description Text (12):
A via in a semiconductor device is created by preparing a starting device having a plurality of layers including a TEOS layer disposed on a TiN layer and an underlayer of Al. This combination of layers are well-known in the industry and can be prepared using any conventional methodology. The via is produced in a conventional manner by use of a C.sub.2 F.sub.6 /C.sub.4 F.sub.8 /CF.sub.4 plasma to etch the dielectric TEOS layer. An oxidizing plasma of O.sub.2 was then used to remove photoresist and organic residues. The resulting starting device is placed in a conventional Reactive Ion Etching (RIE), oxide chamber and evacuated in preparation for the cleaning process accomplished by a plasma etching process. Water vapor is provided to supply OH/H reactive species as an OH/H containing plasma at a flow rate of 350 sccm for 30 seconds at a pressure of 100 mTorr with a bias power of 200 watts for the OH/H containing plasma. Subsequently, a fluorine-based gas of tetrafluoromethane was applied at 50 sccm for 30 seconds at a pressure of 100 mTorr and a bias power of a 200 watts. The resulting via was observed under a microscope to be free of any residues and virtually free of visible breakdown or porosity of the via sidewall.

CLAIMS:

1. A method of cleaning a via which has been formed in a low-k layer of semiconductor material being processed, the method comprising steps of: applying a plasma containing an OH species and an H species to the via in the layer of semiconductor material at a first flow rate of approximately 350 sccm; and subsequently applying a mixture plasma of an oxygen component and a fluorine-based component to the via, the fluorine-based component being a provided at a second flow rate of approximately 50

sccm.